Vivekananda College of Engineering & Technology,Puttur [A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]						
CRM08	Rev 1.10	EC	11/28/20			

CONTINUOUS INTERNAL EVALUATION- 2

Dept:EC	Sem / Div:III A&B	Sub:Digital System Design	S Code:18EC34					
Date:02-12-2020	Time: 2:30-4:00 pm	Max Marks: 50	Elective:N					
Note: Answer any 2 full questions, choosing one full question from each part.								

	Q	Questions	Marks	RBT	COs				
H	N	PART A							
1	a	Define magnitude comparator. Design a combinational circuit that compares two 2-bit binary number and provides 3 outputs	10	L3	CO2				
	b	Explain Master Slave JK flip-flop with the help of circuit diagram and waveforms	8	L2	CO1,3				
	c	Explain 4-bit binary ripple counter.	7	L2	CO1,3				
		OR							
2	a	Design full adder and full subtractor using 74138	8	L3	CO1				
	b	Explain universal shift register.	10	L2	CO1,3				
	c	Explain SR latch as a switch debouncer.	7	L2	CO1,3				
	PART B								
3	a	Implement the function $f(a,b,c,d) = \Sigma m(0,1,3,4,8,9,15)$ using: a) 4:1 mux with a c as select lines	8	L3	CO2				
		b) 8:1 mux with a b.d as select lines							
	b	Design 4 to 16 decoder using 3 to 8 decoder(74138) and Realize the function: a) $P=f(w,x,v,z)=\Sigma(1,4,8,13)$	10	L2	CO1				
		b) $Q=f(a,b,c,d)=\Sigma(2,7,13,15)$							
	c	Find characteristic equation for SR flip-flop and JK flipflop with the help of function table.	7	L2	CO1,3				
	OR								
4	a	Define encoder. Design 4-bit priority encoder with validity output	10	L3	CO2				
	b	Explain the concept of Twisted Ring counter with neat circuit diagram	7	L2	CO1,3				
	c	Explain 4-bit synchronous binary up counter.	8	L2	CO1,3				

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